



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,629	01/27/2004	Glenn Joseph Leedy	ELM-1CONT.15	3771
1473	7590	11/14/2005	EXAMINER	
FISH & NEAVE IP GROUP ROPES & GRAY LLP 1251 AVENUE OF THE AMERICAS FL C3 NEW YORK, NY 10020-1105			HO, TU TU V	
			ART UNIT	PAPER NUMBER
			2818	

DATE MAILED: 11/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	10/766,629	LEEDY, GLENN JOSEPH <i>(initials)</i>
	Examiner Tu-Tu Ho	Art Unit 2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 15 August 2005.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 102-108,117-120,138-147,183-193 and 216-226 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 102-108,117-120,138-147,183-193 and 216-226 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 15 August 2005 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____.   |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____. | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|  | 6) <input type="checkbox"/> Other: _____.                                   |

**DETAILED ACTION**

1. Applicant's Amendment filed 08/15/2005 has been reviewed and placed of record in the file.

***Information Disclosure Statement***

2. Sheet 1 of 2 of the IDS filed 09/10/2004 was not properly initialed by the examiner. The references in the sheet has been considered and properly initialed.

***Drawings***

3. The replacement drawings were received on 08/15/2005. These drawings are accepted.

***Allowable Subject Matter***

4. Prosecution on the merits of this application is reopened on claims 102-108, 117-120, 138-147, 183-193, and 216-226. The indicated allowability of claims 102-108, 117-120, 138-147, 183-193, and 216-226 is withdrawn in view of the newly discovered reference(s) to Copending Application 10/385,386 and Fueki et al. U.S. Patent 5,144,142. Rejections based on the newly cited reference(s) follow.

***Double Patenting***

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686

Art Unit: 2818

F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 102-108, 117-120, 138-147, 183-193, and 216-226 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 113-125 and 183-204, amended 10/28/2005, of copending Application No. 10/385,386 (hereinafter the '386 application). Although the conflicting claims are not identical, they are not patentably distinct from each other.

Referring to **claim 102**, which recites:

An apparatus for forming a patterned layer during manufacture of an integrated circuit, comprising:  
an elastic integrated circuit;  
a plurality of exposure elements; and  
means for selectively irradiating with at least one type of radiant energy portions of a surface of a layer by electronically controlling individually each of the exposure elements.

**Claim 120** of the '386 application discloses:

A lithography tool comprising:  
an array of radiation source cells with apertures formed on a substrate, each radiation source cell for irradiating areas of a surface to be exposed; and  
control circuitry integrated with the substrate for individually controlling each radiation source cell.  
And furthermore, **claim 190** recites at least one elastic dielectric layer.

Comparing present claim 102 and claim 120 of the '386 application, claim 120 does not recite an elastic integrated circuit. Nevertheless, as the elastic integrated circuit of claim 102 constitutes the apparatus and as the control circuitry of claim 120 also constitutes the apparatus, the control circuitry is functionally equivalent to the integrated circuit. As for the limitation "elastic", because Applicant has not particularly defined "elastic integrated circuit" in the

specification, "elastic" is interpreted broadly to be an inherent characteristic of dielectric parts of the integrated circuit; and as such, the control circuitry, which is an integrated circuit, specially wherein the control circuitry integrated with the substrate as claimed in claim 120, shall comprise at least a dielectric component so as to electrically insulate the various metal elements in order for the integrated circuit to individually control each radiation source cell of the array of radiation source cells as claimed; and as such, the apparatus of claim 120 is functionally the same as that of claim 102. Similarly to claim 120, the lithography pattern generation of claim 114 is functionally the same as the apparatus of present claim 102.

As for independent claims, the following are found to be the same or substantially the same:

Present Invention	The '386 reference
103	124-125
104	124-125
105-106	114
117-118	185-186
119-120	190-191
138-139	142
145	143
183	184
184-187	187-189
188-189	196-197
190	199
191	198
192-193	product-by-process limitations
216	184
217-220	187-189
221-222	196-197
223	199
224	198
225-226	product-by-process limitations

For the limitations of claims 107-108 and 140-144, which the claims of the '386 application do not recite, the limitations were deemed to be within routine skills of one of ordinary skill in the art at the time the invention was made to provide.

With respect to claims 146-147, as the lithography tool of claim 120 comprises a control circuitry – which is an integrated circuit - integrated with the substrate for individually controlling each radiation source cell, it would be obvious to further include another dielectric layer, similar to the dielectric material in claims 138 and 145 simply so as to maintain a low inventory (of similar materials for similar use), because at the time the invention was made it was known that integrated circuits comprised multiple layers of metalization interlaced with multiple layers of dielectric for the purpose of saving space.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

#### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- (e) the invention was described in
  - (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
    - (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. **Claims 102-107 and 119** are rejected under 35 U.S.C. 102(e) as being anticipated by Fueki et al. U.S. Patent 5,144,142 (cited by Applicant, and hereinafter referred to as the ‘142 reference).

The ‘142 reference discloses the figures, particularly in Figures 2, 3-4, 7, and 17, and respective portions of the specification an apparatus for forming a patterned layer during manufacture of an integrated circuit as claimed. In particular, the ‘142 reference discloses a blanking aperture array for use in a charged particle beam exposure apparatus for forming a patterned layer during manufacture of an integrated circuit, wherein the aperture array is formed in a substrate, each of the aperture of the array of the apertures comprises a pair of electrodes and associated control shift registers (Abstract).

Referring to **claim 102**, the reference discloses an apparatus for forming a patterned layer during manufacture of an integrated circuit, comprising:

an elastic integrated circuit (generally indicated at 19A, Figs. 4, where “elastic” is interpreted broadly to be an inherent characteristic of dielectric parts of the integrated circuit, dielectric parts such as 98, 103, (Figs. 4B, 4C, column 10, lines 5-15), SiO<sub>2</sub> layer or the like (Figs. 17’s, column 17, lines 15-20) );

a plurality of exposure elements (generally indicated at, for example, the elements 92/97/98/94 (electrodes and dielectric layers that define exposure aperture element 19c, Figs. 4A and 4B; or the elements 102/103/99/104, Fig. 4C); and

means for selectively irradiating with at least one type of radiant energy (electron beam EG, Fig. 2, column 3, lines 30-40) portions of a surface of a layer (generally indicated at wafer WF, Fig. 2) by electronically controlling individually each of the exposure elements (Figs. 2, 3-4, 7, and 17, column 8, lines 12+).

Referring to **claim 103**, the reference further discloses that the radiant energy is electron beam, as noted above.

Referring to **claim 104**, the reference further discloses that the exposure elements are miniature sources of electron beam (electron beam EB, Fig. 4B).

Referring to **claim 105**, the reference further discloses that the exposure elements control passage of radiant energy (EB) from an external source (generally indicated at EG, Fig. 2).

Referring to **claim 106**, the reference further discloses that the exposure elements control passage of radiant energy from an external source using electromagnetic deflection (produced by electrodes 91, 92, 94 or 99, 104, Figs. 4)

Referring to **claim 107**, the reference further discloses means (such as 19A, Figs. 4) for separately focusing radiant energy emitted from the plurality of exposure elements.

Referring to **claim 119**, the reference further discloses an elastic dielectric layer (Figs. 17, where a plurality of un-depicted SiO<sub>2</sub> layer or the like (Figs. 17's, column 17, lines 15-20) are used to insulate electrically conductive electrodes 3's) with "elastic" being interpreted broadly as noted above.

### *Claim Rejections § 102 & § 103*

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. **Claim 108** is rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Fueki et al. U.S. Patent 5,144,142 (the ‘142 reference).

The reference discloses an apparatus for forming a patterned layer during manufacture of an integrated circuit as detailed above for claim 102 and further discloses shifting the plurality of exposure elements with respect to the surface (through means ST, Fig. 2). And although the reference does not explicitly disclose ceasing irradiating the surface and resuming irradiating the surface between a shifting the plurality of exposure elements with respect to the surface as claimed, it appears that ceasing irradiating the surface and resuming irradiating the surface between a shifting the plurality of exposure elements with respect to the surface are required or necessary operations.

***Claim Rejections - 35 USC § 103***

9. **Claim 183** is rejected under 35 U.S.C. §103(a) as being unpatentable over Fueki et al. U.S. Patent 5,144,142 (the ‘142 reference).

The reference discloses an apparatus for forming a patterned layer during manufacture of an integrated circuit as detailed above for claim 102 and further discloses that the plurality of exposure elements includes about 100,000 elements (100 X 1000 aperture elements, column 14, lines 12-20). Although the reference does not disclose at least one million elements as claimed, the reference does not disclose that at least one million elements is not attainable, therefore changing from 100,000 to at least one million would have been obvious to one of ordinary skill in the art at the time the invention was made.

***Allowable Subject Matter***

Art Unit: 2818

10. Claim 117 and dependent claims 118, 184, and 186-193; claim 138 and dependent claims 139-147 and 216-226; claim 120 and dependent claim 185, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and insofar as in compliance with the double patenting rejection noted above.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious an apparatus for forming a patterned layer during manufacture of an integrated circuit having all exclusive limitations as recited in claims 117, 138, and 120, characterized in the stress-controlled dielectric layer as claimed or in the elastic dielectric layer having the stress as claimed.

### *Conclusion*

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2818

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Tu-Tu Ho  
November 02, 2005